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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,924	03/08/2004	Richard M. Fastow	H1807	1784

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THE CAVANAGH LAW FIRM
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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/795,924	FASTOW RICHARD	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 1-22) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 23-31 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-22 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 5,045,490 to Esquivel et al.

Regarding to claim 1, Esquivel discloses a semiconductor component, comprising a substrate 158 having a major surface; a trench 54 having first and second sidewalls

extending from the major surface into the substrate; a first column of memory cells 23 (figs. 1, 5) adjacent the first sidewall; and a trench line disposed in the trench, wherein the trench line is electrically coupled to the first column of memory cells (page 10, and claim 1).

Regarding to claim 2, the semiconductor component of claim 1, wherein the first column of memory cells comprises at least one memory cell having a gate structure, a drain region, and a source region (fig. 1).

Regarding to claim 3, the semiconductor component of claim 2, further including a first connector, wherein the first connector electrically couples one of the source region or the drain region to the trench line (fig. 1).

Regarding to claim 4, the semiconductor component of claim 3, further including a second connector, wherein the second connector electrically couples the other of the source region or the drain region to the trench line (fig. 1).

Regarding to claim 5, the semiconductor component of claim 3, wherein the trench line serves as a bit line (page 10, lines 19-20, fig. 1).

Regarding to claim 6, the semiconductor component of claim 2, further including a drain connector, wherein the drain connector electrically couples the drain region of the at least one memory cell to the trench line (figs. 1 and 5).

Regarding to claim 7, the semiconductor component of claim 6, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line (figs. 1 and 5).

Regarding to claim 8, the semiconductor component of claim 2, further including a source connector, wherein the source connector electrically couples the source region of the at least one memory cell to the trench line (figs. 1 and 5).

Regarding to claim 9, the semiconductor component of claim 8, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region (figs. 1 and 5).

Regarding to claim 10, the semiconductor component of claim 8, further including another drain connector, wherein the another drain connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line (figs. 1 and 5).

Regarding to claim l 1, the semiconductor component of claim 8, further including another source connector, wherein the another source connector electrically couples the drain region of the at least one memory cell of the second column of memory cells to the trench line (figs. 1 and 5).

Regarding to claim 12, the semiconductor component of claim 1, further including a second column of memory cells, wherein the second column of memory cells is adjacent the second sidewall and comprises at least one memory cell having a gate structure, a drain region, and a source region (figs. 1 and 5).

Regarding to claim 13, Esquivel discloses the memory device, comprising a first memory cell having a gate structure, a drain region, and a source region; a second memory cell having a gate structure, a drain region, and a source region, wherein the source region of the second memory cell is coupled to the source region of the first memory cell, and wherein the first and second memory cells cooperate to form a first column of memory cells; and a first trench line adjacent the first column of memory cells, wherein the source regions of the first and second memory cells are coupled to the first trench line (page 10, and claim 1, and figs 1, 5, 8).

Regarding to claim 14, the memory device of claim 13, further including a second trench line adjacent the first column of memory cells, wherein the drain regions of the

first and second memory cells are coupled to the second trench line (claim 1 and figs 5, 8).

Regarding to claim 15 (original), the memory device of claim 14, further including a third memory cell having a gate structure, a drain region, and a source region; and a fourth memory cell having a gate structure, a drain region, and a source region, wherein the source region of the fourth memory cell is coupled to the source region of the third memory cell and the source regions of the third and fourth memory cells are coupled to the second trench line, and wherein the third and fourth memory cells cooperate to fonn a second column of memory cells (claim 1, fig. 1, 5, 8).

Regarding to claim 16, the memory device of claim 15, wherein the second trench line is between the first and second columns of memory cells (figs. 1, 5, 8).

Regarding to claim 17, the memory device of claim 15, further including a third trench line adjacent the second column of memory cells (figs. 1, 5, 8).

Regarding to claim 18, the memory device of claim 17, wherein the drain regions of the third and fourth memory cells are coupled to the third trench line (figs. 1, 5, 8).

Regarding to claim 19, the memory device of claim 18, wherein the first trench line serves as a first bit line, the second trench line serves as a second bit line, and the third trench line serves as a third bit line (claim 1, and figs. 1, 5, 8).

Regarding to claim 20, the memory device of claim 15, further including a first bit line coupled to the drain regions of the first and second memory cells (fig 1).

Regarding to claim 21, the memory device of claim 20, further including a second bit line coupled to the drain regions of the second and third memory cells (fig. 1).

Regarding to claim 22, the memory device of claim 13, further including a first bit line coupled to the drain regions of the first and second memory cells (fig. 1).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MH

Mai-Huong Tran